CLAIMS

What is claimed is:

1. A highly linear power amplifier comprises:

component;

first transistor pair coupled in series with the component, wherein a first transistor of the first transistor pair is coupled to receive an input signal and wherein a second transistor of the first transistor pair is coupled to receive a first enable signal; and

second transistor pair coupled in series with the component, wherein a first transistor of the second transistor pair is coupled to receive the input signal, wherein a second transistor of the second transistor pair is coupled to receive a second enable signal, wherein when the first enable signal is enabled the highly linear power amplifier has a first gain with a first linearity and when the second enable signal is enabled the highly linear power amplifier has a second gain with the first linearity.

2. The highly linear power amplifier of claim 1, wherein the component comprises at least one of: a resistor, an inductor, and a linearly loaded transistor.

3. The highly linear power amplifier of claim 1 further comprises:

at least one other transistor pair coupled in series with the component, wherein a first transistor of the at least one other transistor pair is coupled to receive the input signal, wherein a second transistor of the at least one other transistor pair is coupled to receive at least one other enable signal, and wherein when the at least one other enable signal is enabled the highly linear power amplifier has at least one other gain with the first linearity.

4. The highly linear power amplifier of claim 1 further comprises:

the first transistor of the first transistor pair has a first size to produce the first gain; and

the first transistor of the second transistor pair has a second size to produce the second gain, wherein the first size is greater than the second size by a desired ratio such that first gain is greater than the second gain by the desire ratio.

5. The highly linear power amplifier of claim 1 further comprises:

second component;

first complimentary transistor pair coupled in series with the second component, wherein a first transistor of the first complimentary transistor pair is coupled to receive a

complimentary input signal and wherein a second transistor of the first complimentary transistor pair is coupled to receive the first enable signal; and

second complimentary transistor pair coupled in series with the second component, wherein a first transistor of the second complimentary transistor pair is coupled to receive the complimentary input signal, wherein a second transistor of the second complimentary transistor pair is coupled to receive the second enable signal.

6. The highly linear power amplifier of claim 1 further comprises:

control module operably coupled to generate the first and second enable signals based on desired output levels of the highly linear power amplifier.

7. The highly linear power amplifier of claim 6, wherein the control module further comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

determine a first desired output level of the highly linear power amplifier and consequently enable the second enable signal such that the highly linear power amplifier has the second gain;

determine a second desired output level of the highly linear power amplifier and consequently enable the first enable signal such that the highly linear power amplifier has the first gain, wherein the first gain is greater than the second gain; and

determine a third desired output level of the highly linear power amplifier and consequently enable the first and second enable signals such that the highly linear power amplifier has a cumulative gain of the first and second gains, wherein the cumulative gain is greater than the first gain.

8. A linear transmitter comprises:

processing module;

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

determine an output power level of an outbound radio frequency (RF) signal; and

enable at least one of a first enable signal and a second enable signal based on the determined output power level;

up-conversion module operably coupled to produce an RF signal from an I component of a low intermediate frequency (IF) outbound signal, a Q component of the low IF outbound signal, an I component of a local oscillation, and a Q component of the local oscillation;

highly linear power amplifier operably coupled to produce an amplified RF signal by amplifying the RF signal based on at least one of: a first enable signal and a second enable signal, wherein the highly linear power amplifier includes:

component;

first transistor pair coupled in series with the component, wherein a first transistor of the first transistor pair is coupled to receive the RF signal and wherein a second transistor of the first transistor pair is coupled to receive the first enable signal; and

second transistor pair coupled in series with the component, wherein a first transistor of the second transistor pair is coupled to receive the RF signal, wherein a second transistor of the second transistor pair is coupled to receive the second enable signal, wherein when the first enable signal is enabled the highly linear power amplifier has a first gain with a first linearity and when the second enable signal is enabled the highly linear power amplifier has a second gain with the first linearity; and

output power amplifier operably coupled to produce the outbound RF signal by further amplifying the amplified RF signal.

9. The linear transmitter of claim 8, wherein the output power amplifier includes:

second component;

third transistor pair coupled in series with the second component, wherein a first transistor of the third transistor pair is coupled to receive the amplified RF signal and

wherein a second transistor of the third transistor pair is coupled to receive a third enable signal; and

fourth transistor pair coupled in series with the second component, wherein a first transistor of the fourth transistor pair is coupled to receive the amplified RF signal, wherein a second transistor of the fourth transistor pair is coupled to receive a fourth enable signal, wherein processing module generates at least one of the third enable signal and the fourth enable signal based, at least in part, on the desired output level.

10. The linear transmitter of claim 8, wherein the highly linear power amplifier further comprises:

at least one other transistor pair coupled in series with the component, wherein a first transistor of the at least one other transistor pair is coupled to receive the RF signal, wherein a second transistor of the at least one other transistor pair is coupled to receive at least one other enable signal, and wherein when the at least one other enable signal is enabled the highly linear power amplifier has at least one other gain with the first linearity.

11. The linear transmitter of claim 8, wherein the highly linear power amplifier further comprises:

second component;

first complimentary transistor pair coupled in series with the second component, wherein a first transistor of the first complimentary transistor pair is coupled to receive a complimentary RF signal and wherein a second transistor of the first complimentary transistor pair is coupled to receive the first enable signal; and

second complimentary transistor pair coupled in series with the second component, wherein a first transistor of the second complimentary transistor pair is coupled to receive the complimentary signal, wherein a second transistor of the second complimentary transistor pair is coupled to receive the second enable signal.

12. A radio comprising:

receiver operably coupled to convert an inbound RF signal into an I component of an inbound low intermediate frequency (IF) signal and a Q component of the low IF signal based on an I component of a receiver local oscillation and a Q component of the receiver local oscillation; and

transmitter that includes:

processing module;

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

determine an output power level of an outbound radio frequency (RF) signal; and

enable at least one of a first enable signal and a second enable signal based on the determined output power level;

up-conversion module operably coupled to produce an RF signal from an I component of a low intermediate frequency (IF) outbound signal, a Q component

of the low IF outbound signal, an I component of a local oscillation, and a Q component of the local oscillation;

highly linear power amplifier operably coupled to produce an amplified RF signal by amplifying the RF signal based on at least one of: a first enable signal and a second enable signal, wherein the highly linear power amplifier includes:

component;

first transistor pair coupled in series with the component, wherein a first transistor of the first transistor pair is coupled to receive the RF signal and wherein a second transistor of the first transistor pair is coupled to receive the first enable signal; and

second transistor pair coupled in series with the component, wherein a first transistor of the second transistor pair is coupled to receive the RF signal, wherein a second transistor of the second transistor pair is coupled to receive the second enable signal, wherein when the first enable signal is enabled the highly linear power amplifier has a first gain with a first linearity and when the second enable signal is enabled the highly linear power amplifier has a second gain with the first linearity; and

output power amplifier operably coupled to produce the outbound RF signal by further amplifying the amplified RF signal.

13. The radio of claim 12, wherein the output power amplifier includes:

second component;

third transistor pair coupled in series with the second component, wherein a first transistor of the third transistor pair is coupled to receive the amplified RF signal and wherein a second transistor of the third transistor pair is coupled to receive a third enable signal; and

fourth transistor pair coupled in series with the second component, wherein a first transistor of the fourth transistor pair is coupled to receive the amplified RF signal, wherein a second transistor of the fourth transistor pair is coupled to receive a fourth enable signal, wherein processing module generates at least one of the third enable signal and the fourth enable signal based, at least in part, on the desired output level.

14. The radio of claim 12, wherein the highly linear power amplifier further comprises:

at least one other transistor pair coupled in series with the component, wherein a first transistor of the at least one other transistor pair is coupled to receive the RF signal,

wherein a second transistor of the at least one other transistor pair is coupled to receive at least one other enable signal, and wherein when the at least one other enable signal is enabled the highly linear power amplifier has at least one other gain with the first linearity.

15. The radio of claim 12, wherein the highly linear power amplifier further comprises:

second component;

first complimentary transistor pair coupled in series with the second component, wherein a first transistor of the first complimentary transistor pair is coupled to receive a complimentary RF signal and wherein a second transistor of the first complimentary transistor pair is coupled to receive the first enable signal; and

second complimentary transistor pair coupled in series with the second component, wherein a first transistor of the second complimentary transistor pair is coupled to receive the complimentary signal, wherein a second transistor of the second complimentary transistor pair is coupled to receive the second enable signal.

16. A differential highly linear power amplifier comprises:

first component;

second component;

first differential enable transistor pair operably coupled to the first and second components, wherein the first differential enable transistor pair is operably coupled to receive a first enable signal;

first differential input transistor pair operably coupled to the first differential enable transistor pair, wherein the first differential input transistor pair is operably coupled to receive a differential input signal;

second differential enable transistor pair operably coupled to the first and second components, wherein the second differential enable transistor pair is operably coupled to receive a second enable signal; and

second differential input transistor pair operably coupled to the second differential enable transistor pair, wherein the second differential input transistor pair is operably coupled to receive the differential input signal.

17. The differential highly linear power amplifier of claim 16, wherein the first differential enable transistor pair, the first differential input transistor pair, the second differential enable transistor pair, and the second differential input transistor pair comprise at least one of:

P-channel transistors; and

N-channel transistors.

18. The differential highly linear power amplifier of claim 16 further comprises:

third differential enable transistor pair operably coupled to the first and second components, wherein the third differential enable transistor pair is operably coupled to receive a third enable signal; and

third differential input transistor pair operably coupled to the third differential enable transistor pair, wherein the third differential input transistor pair is operably coupled to receive the differential input signal.